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S/N 10/719,921

REMARKS**DEC 05 2006****I. Status of the Application.**

In the Office Action mailed June 14, 2006: (1) Claim 4 was objected to because of a minor informality, which has been corrected in the above-amendments; and
5 (2) Claims 1- 32 were rejected under 35 U.S.C. §102(e) as being anticipated by Scheuermann U.S. Patent Application Publication No. 2004/0015970 ("Scheuermann" or the "Scheuermann reference").

Upon entry of this amendment, claims 1, 3 - 7, 9, 10, 12 - 27 and 29 - 32 remain pending. Support for the amendments may be found in the cancelled dependent
10 claims. In addition, various claims have been amended to utilize more formal language, such as "memory processing circuit" rather than "engine", "circuit" rather than "machine", and "retrieve/write" rather than the more colloquial "peek/poke". Support for these amendments may be found throughout the specification. No new matter has been introduced.

15 Applicants respectfully traverse the rejection of the various claims under Section 102, and respectfully request reconsideration of the pending claims in view of the foregoing amendments and the following remarks.

II. The Rejection of Claims 1-32 under 35 U.S.C. §102(e) Should Be Withdrawn.

20 The present invention as claimed is not disclosed and is not suggested by the Scheuermann reference. Scheuermann pertains to data flow control, using task parameters and a finite state machine, and has nothing to do with the memory controller of the present invention, which interfaces between an adaptive computing circuit and an external memory. Nothing in the Scheuermann reference discloses or suggests each and
25 every feature of the independent claims and, therefore, the present invention is not anticipated and is not rendered obvious by the Scheuermann reference.

Indeed, the only memory discussion in Scheuermann is quite general, indicating only a "system memory 1008" and "bulk memory interfaces to high performance memory controllers and associated memories 1004" in Figure 1 and a
30 "network memories 1024 and data memories 1026" in Figure 2. There is no disclosure or suggestion in Scheuermann concerning any of the claimed elements of the present

S/N 10/719,921

invention, such as claimed in claim 1: (1) a network interface configured to receive a memory request from the programmable network and to send data to and receive data from the programmable network; (2) a memory interface configured to access a memory to fulfill the memory request; and (3) at least one memory processing circuit coupled to the network interface and to the memory interface, the memory processing circuit configured to provide a memory access service of a plurality of memory access services, wherein the memory interface receives and provides data for the memory request using the memory access service.

Similarly, there is no disclosure or suggestion of any kind in the Scheuermann reference which is relevant to the claimed invention as claimed in the other independent claims. More specifically, nothing in Scheuermann discloses or suggests:

(1) In independent claim 6, "a memory processing circuit configured to receive the memory request and to provide a memory access service of a plurality of memory access services, the memory access service associated with the memory request, and wherein the plurality of memory access services comprise at least one of a retrieve/write ("peek/poke") service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service."

(2) In independent claim 10, (a) one or more ports configured to receive memory requests, wherein each port includes one or more parameters; (b) a memory processing circuit configured to receive a memory request from a port in the one or more ports; and (c) a data address generator configured to generate a memory location for a memory based on the one or more parameters associated with the port, wherein (d) the memory processing circuit is further configured to perform a memory operation for the memory request using the generated memory location, the memory processing circuit comprising a processing circuit to perform at least one of point-to-point memory requests, direct memory access memory requests, and real-time input memory requests.

(3) In independent claim 18, (a) one or more ports configured to receive memory requests from requesting nodes, wherein each port includes one or more parameters, the one or more parameters configurable by information in the memory requests; (b) a data address generator configured to generate a memory location for a

S/N 10/719,921

memory based on the one or more parameters associated with the port; and (c) a point-to-point engine configured to receive a memory request from a port in the one or more ports and to perform a memory operation using the generated memory location while adhering to a point-to-point protocol with the requesting node.

- 5 (4) In independent claim 27, (a) one or more nodes configured to generate a memory service request; and (b) a memory controller configured to receive the memory service request, the memory controller configured to service the memory service request by reading data from or writing data to the memory based on the memory service request, and the memory controller further configured to provide at least one of a
10 retrieve/write ("peek/poke") service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service.

Indeed, there is no disclosure of any kind in Scheuermann concerning any type of memory access. Reviewing each and every sentence and paragraph in the
15 Scheuermann reference reveals the following:

1. Paragraphs 1 – 3 provide general background on the need for data flow control and control of task execution.
2. The summary section, paragraphs 4 and 5, pertain to associating task parameters with tasks of an execution node, with the readiness of task resources
20 based on task parameters, and the use of data flow techniques.
3. Paragraphs 6 – 9 identify the drawings.
4. Paragraph 10 describes the Scheuermann invention as relating to data flow control during task execution, and that the Scheuermann invention is not to be limited to the illustrated embodiments.
- 25 5. Paragraph 11 indicates only a "system memory 1008" and "bulk memory interfaces to high performance memory controllers and associated memories 1004", with no discussion of the operation of any type of memory controller.
6. Paragraph 12 of Scheuermann generally discusses data flow within the
30 system of Figure 2, referring to "network memories 1024 and data memories 1026", with no discussion of the operation of any type of memory controller.

S/N 10/719,921

7. Paragraphs 13 and 14 of Scheuermann generally discuss a node having input and output ports, with finite state machine-controlled execution units, with task parameters to determine when a task is ready for execution, and also with no discussion of the operation of a memory controller of any kind.

5 8. Paragraph 15 of Scheuermann generally discusses determining the status of task parameters using flags and lookup tables, with no discussion of the operation of any type of memory controller.

9. Paragraph 16 of Scheuermann generally discusses that data flow control may be used for pacing of task execution, also with no discussion of the operation of any type of memory controller.

10 10. Paragraph 17 of Scheuermann discusses that the Scheuermann invention is defined by the claims, with the balance of the Scheuermann reference consisting of 23 claims, with no discussion of the operation of any memory controller of any kind.

15 Clearly and indisputably, nothing in the Scheuermann reference discloses or suggests the present invention. As a consequence, the Scheuermann reference does not disclose and does not suggest each and every claimed feature of the present invention. Accordingly, present invention as claimed is not anticipated by and is not rendered
20 obvious by Scheuermann. Applicants respectfully request, therefore, that the Patent Office withdraw the section 102(e) rejection of the pending claims.

It is well-established law that all claimed elements must be found in the prior art for anticipation to be found. *See, e.g.,* MPEP §706.02. "For a prior art reference to anticipate a claim, the reference must disclose each and every element of the claim
25 with sufficient clarity to prove its existence in the prior art...[and] that presumed knowledge does not grant a license to read into the reference teachings that are not there". *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 43 USPQ2D1481, 1490 (Fed. Cir. 1997). Accordingly, the claimed features and teachings of the present invention are not to be "read" into the Scheuermann reference, and such reading of the present
30 invention into the prior art is impermissible "hindsight."

S/N 10/719,921

It is also well-established law that the Patent Office may not rely upon factually unsupported conclusions, in the Office Action, that the claimed features of the present invention are "necessarily" or somehow "inherently" in the Scheuermann reference when these claimed features are not, in fact, in that reference or any other reference. The Patent Office is required to literally "point to the 'page and line' of the prior art" to justify any claim of inherency. *Glaxo Inc. v. Novopharm Ltd.*, 29 USPQ2d 1126, 1128 (E.D.N.C. 1993), citing *Stoller v. Ford Motor Co.*, 18 USPQ2d 1545, 1547 (Fed. Cir. 1991) and *In re Sovish*, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985), *aff'd*, 52 F.3d 1043, 34 USPQ2d 1565, 1569 (Fed. Cir.), *cert. denied*, 516 U.S. 988 (1995). The Patent Office has not met this burden and, accordingly, the rejection of the pending claims must be withdrawn.

As a consequence, the cited reference does not disclose and does not suggest the present invention. The present invention, therefore, is not anticipated (and is not rendered obvious by) the reference under Section 102 (and Section 103), and the rejection of the claims should be withdrawn. In addition, because the remaining dependent claims incorporate by reference all of the limitations of the corresponding independent claims, all of the dependent claims are also allowable over the cited references.

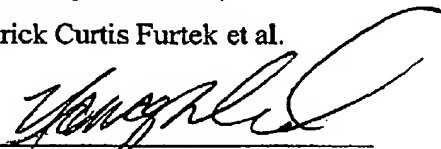
On the basis of the above amendments and remarks, reconsideration and allowance of the application is believed to be warranted, and an early action toward that end is respectfully solicited. In addition, for any issues or concerns, the Examiner is invited to call the attorney for the applicant at the telephone number provided below.

Respectfully submitted,

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December 5, 2006

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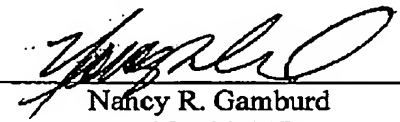
S/N 10/719,921

DEC 05 2006

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment And Response Under 37
CFR 1.111 And 1.115 (13 pages), Transmittal (PTO/SB/21) (1 page), Fee Transmittal
5 (PTO/SB/17) (1 page), and Petition for Extension of Time (PTO/SB/22) (2 pages,
original plus 1 copy) (17 pages total), for Frederick Curtis Furtek et al., Serial No.
10/719,921, entitled "External Memory Controller Node", have been transmitted by
facsimile to the US Patent and Trademark Office to fax number (571) 273-8300
(Centralized Facsimile Number), on December 5, 2006.

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